

WHAT IS CLAIMED IS:

- 1 1. A power supply comprising:
2 a buck regulator coupled to a regulator input voltage and generating a
3 regulated output voltage for powering a load referenced to a first ground potential in
4 response to an ON-time voltage pulse, wherein said ON-time voltage pulse has a first
5 logic state when said regulated output voltage supplies energy to said load directly
6 from said regulator input and a second logic state when said regulated output voltage
7 is supplying energy stored from said regulator input voltage;
8 a controller for generating said ON-time voltage pulse in response to said
9 regulator input voltage, said regulated output voltage, and a compensated reference
10 voltage;
11 a reference circuit having an reference output generating a modified reference
12 voltage relative to said first ground potential in response to a reference input voltage
13 generated relative to a second ground potential; and
14 compensated reference circuitry for generating said compensated reference
15 voltage as a time integral of a difference between said modified reference voltage and
16 said regulator output voltage multiplied times a gain factor.
- 1 2. The power supply of claim 1, wherein said first and second ground potentials
2 are equal potentials.
- 1 3. The power supply of claim 2, wherein a pulse width of said ON-time voltage
2 pulse is generated in response to comparing said compensated reference to said
3 regulated output voltage.

1 4. The power supply of claim 2, wherein said difference between said modified
2 reference voltage and said regulator output voltage multiplied times said gain factor is
3 limited to a value between a maximum positive value and a maximum negative value.

1 5. The power supply of claim 2, wherein said compensated reference circuitry
2 comprises a reference amplifier having an input coupled to said reference input
3 voltage and an amplifier output coupled to said reference output, said amplifier output
4 generating said reference input voltage multiplied by said gain factor.

1 6. The power supply of claim 2, wherein said compensated reference circuitry
2 comprises:

3 a reference amplifier having an input coupled to said reference input voltage
4 and an amplifier output generating said reference input voltage multiplied by said
5 gain factor; and

6 a digital to analog converter (DAC) having a DAC reference input coupled to
7 said amplifier output, a plurality of digital input signals, and a DAC output coupled to
8 said reference output.

1 7. The power supply of claim 1, wherein a pulse width of said ON-time voltage
2 pulse is generated in response to comparing said compensated reference to said
3 regulated output voltage.

1 8. The power supply of claim 1, wherein said difference between said modified
2 reference voltage and said regulator output voltage multiplied times said gain factor is
3 limited to a value between a maximum positive value and a maximum negative value.

1 9. The power supply of claim 1, wherein said compensated reference circuitry
2 comprises:

3 a reference amplifier having an input coupled to said reference input voltage
4 and an amplifier output coupled to said reference output, said amplifier output
5 generating said reference input voltage multiplied by said gain factor;

6 a voltage to current converter having an input coupled to said amplifier output
7 and a current output generating a current proportional to said reference input voltage
8 multiplied by said gain factor; and

9 a resistor having a first terminal coupled to said first ground potential and a
10 second terminal coupled to said current output and said reference output, wherein said
11 modified reference is generated relative to said first ground potential.

1 10. The power supply of claim 9, further comprising a capacitor coupled across
2 said resistor.

1 11. The power supply of claim 1, wherein said compensated reference circuitry
2 comprises:

3 a reference amplifier having an input coupled to said reference input voltage
4 and an amplifier output, said amplifier output generating said reference input voltage
5 multiplied by said gain factor;

6 a digital to analog converter (DAC) having a DAC reference input coupled to
7 said amplifier output, a plurality of digital input signals, and a DAC output generating
8 a DAC voltage proportional to said reference input voltage multiplied by said gain
9 factor in response to logic states of said digital input signals;

10 a voltage to current converter having an input coupled to said DAC output and
11 a current output generating a current proportional to said DAC voltage; and

12 a resistor having a first terminal coupled to said first ground potential and a
13 second terminal coupled to said current output and said reference output, wherein said
14 modified reference is generated relative to said first ground potential.

1 12. The power supply of claim 11, further comprising a capacitor coupled across
2 said resistor.

1 13. The power supply of claim 1, wherein said compensated reference circuitry
2 comprises;

3 transconductance amplifier having a gain G_m , a positive input coupled to said
4 modified reference voltage, a negative input coupled to said regulator output voltage,
5 and slew current output generating a slew current proportional to a difference
6 between said modified reference voltage and said regulator output voltage times said
7 gain G_m ; and

8 a capacitor having a capacitance C_m , a first terminal coupled to said second
9 ground potential and a second terminal coupled to said slew current output, wherein a
10 voltage across said capacitor generates said compensated reference voltage and said
11 gain factor is said gain G_m times said capacitance C_m .

1 14. A system comprising:
2 a processor referenced to a first ground potential;
3 a memory for storing instructions and data for said processor;
4 a power supply having a buck regulator coupled to a regulator input voltage
5 and generating a regulated output voltage coupled to said processor in response to an
6 ON-time voltage pulse wherein said ON-time voltage pulse has a first logic state
7 when said regulated output voltage supplies energy to said processor directly from
8 said regulator input and a second logic state when said regulated output voltage is
9 supplying energy stored from said regulator input voltage;
10 a controller for generating said ON-time voltage pulse in response to said
11 regulator input voltage, said regulated output voltage, and a compensated reference
12 voltage;
13 a reference circuit having an reference output generating a modified reference
14 voltage relative to said first ground potential in response to a reference input voltage
15 generated relative to a second ground potential; and
16 compensated reference circuitry for generating said compensated reference
17 voltage as a time integral of a difference between said modified reference voltage and
18 said regulator output voltage multiplied times a gain factor.

1 15. The system of claim 14, wherein said first and second ground potentials are
2 equal potentials.

1 16. The system of claim 15, wherein a pulse width of said ON-time voltage pulse
2 is generated in response to comparing said compensated reference to said regulated
3 output voltage.

1 17. The system of claim 15, wherein said difference between said modified
2 reference voltage and said regulator output voltage multiplied times said gain factor is
3 limited to a value between a maximum positive value and a maximum negative value.

1 18. The system of claim 15, wherein said compensated reference circuitry
2 comprises a reference amplifier having an input coupled to said reference input
3 voltage and an amplifier output coupled to said reference output, said amplifier output
4 generating said reference input voltage multiplied by said gain factor.

1 19. The system of claim 15, wherein said compensated reference circuitry
2 comprises:

3 a reference amplifier having an input coupled to said reference input voltage
4 and an amplifier output generating said reference input voltage multiplied by said
5 gain factor; and

6 a digital to analog converter (DAC) having a DAC reference input coupled to
7 said amplifier output, a plurality of digital input signals, and a DAC output coupled to
8 said reference output.

1 20. The system of claim 14, wherein a pulse width of said ON-time voltage pulse
2 is generated in response to comparing said compensated reference to said regulated
3 output voltage.

1 21. The system of claim 14, wherein said difference between said modified
2 reference voltage and said regulator output voltage multiplied times said gain factor is
3 limited to a value between a maximum positive value and a maximum negative value.

1 22. The system of claim 14, wherein said compensated reference circuitry
2 comprises:

3 a reference amplifier having an input coupled to said reference input voltage
4 and an amplifier output coupled to said reference output, said amplifier output
5 generating said reference input voltage multiplied by said gain factor;

6 a voltage to current converter having an input coupled to said amplifier output
7 and a current output generating a current proportional to said reference input voltage
8 multiplied by said gain factor; and

9 a resistor having a first terminal coupled to said first ground potential and a
10 second terminal coupled to said current output and said reference output, wherein said
11 modified reference is generated relative to said first ground potential.

1 23. The system of claim 22, further comprising a capacitor coupled across said
2 resistor.

1 24. The system of claim 14, wherein said compensated reference circuitry
2 comprises:

3 a reference amplifier having an input coupled to said reference input voltage
4 and an amplifier output, said amplifier output generating said reference input voltage
5 multiplied by said gain factor;

6 a digital to analog converter (DAC) having a DAC reference input coupled to
7 said amplifier output, a plurality of digital input signals, and a DAC output generating
8 a DAC voltage proportional to said reference input voltage multiplied by said gain
9 factor in response to logic states of said digital input signals;

10 a voltage to current converter having an input coupled to said DAC output and
11 a current output generating a current proportional to said DAC voltage; and

12 a resistor having a first terminal coupled to said first ground potential and a
13 second terminal coupled to said current output and said reference output, wherein said
14 modified reference is generated relative to said first ground potential.

1 25. The system of claim 24, further comprising a capacitor coupled across said
2 resistor.

1 26. The system of claim 14, wherein said compensated reference circuitry
2 comprises;

3 transconductance amplifier having a gain G_m , a positive input coupled to said
4 modified reference voltage, a negative input coupled to said regulator output voltage,
5 and slew current output generating a slew current proportional to a difference
6 between said modified reference voltage and said regulator output voltage times said
7 gain G_m ; and

8 a capacitor having a capacitance C_m , a first terminal coupled to said second
9 ground potential and a second terminal coupled to said slew current output, wherein a
10 voltage across said capacitor generates said compensated reference voltage and said
11 gain factor is said gain G_m times said capacitance C_m .